FIG. 1

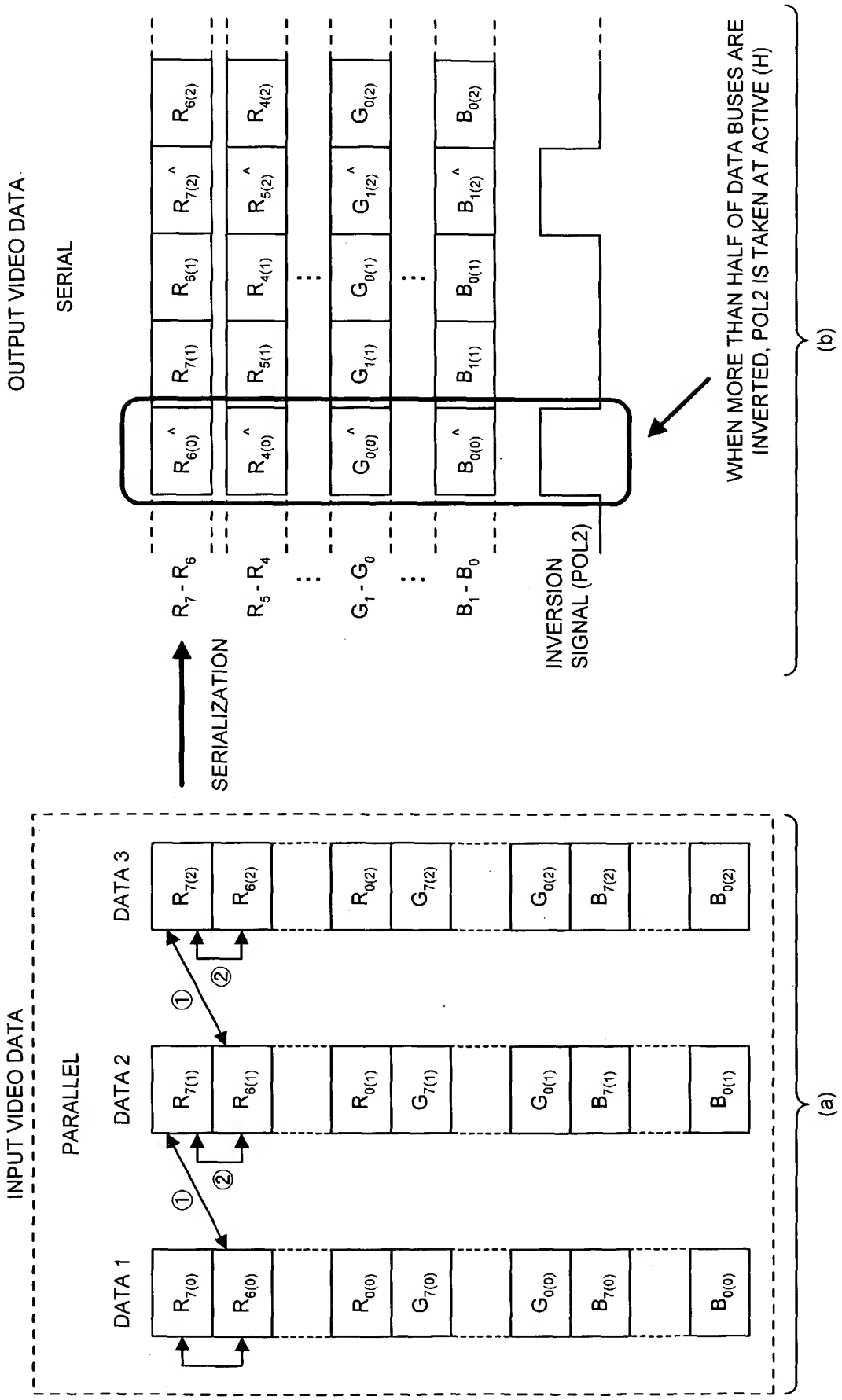
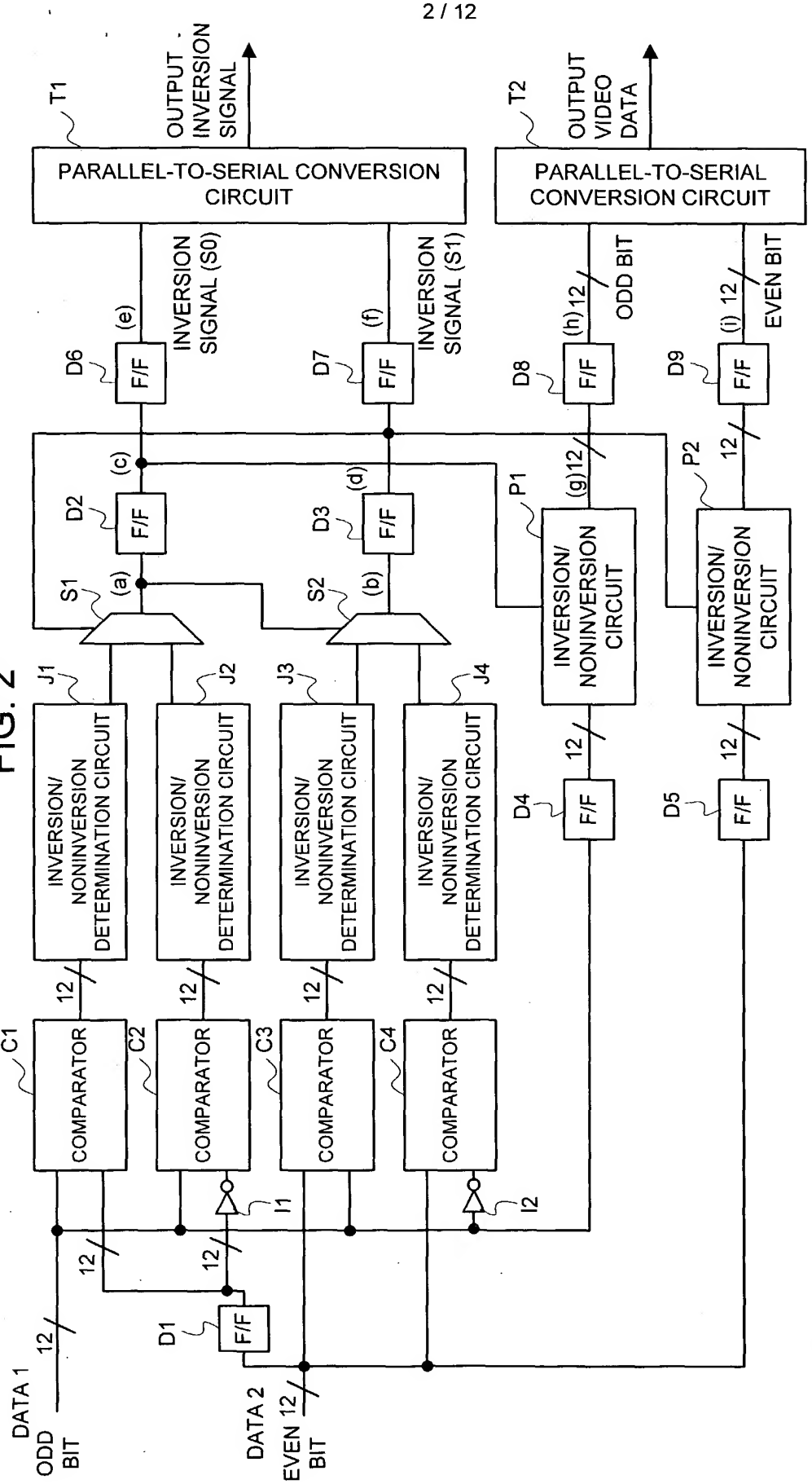

INPUT VIDEO DATA
PARALLEL
DATA 1
DATA 2
DATA 3
(a)
SERIALIZATION
OUTPUT VIDEO DATA
SERIAL
INVERSION SIGNAL (POL2)
WHEN MORE THAN HALF OF DATA BUSES ARE INVERTED, POL2 IS TAKEN AT ACTIVE (H)
(b)

FIG. 2



* IN THIS EXAMPLE, INPUT VIDEO DATA HAS 24 BITS (EACH OF R, G, AND B HAS 8 BITS)
* INVERSION SIGNAL (S0) IS INVERSION SIGNAL FOR ODD BIT, AND INVERSION SIGNAL (S1) IS INVERSION SIGNAL FOR EVEN BIT.
* POINTS (a) TO (f) ARE OBSERVATION POINT OF TIMING CHART OF FIG.2.
* EACH F/F HAS CLOCK AND RESET TERMINAL

FIG. 3

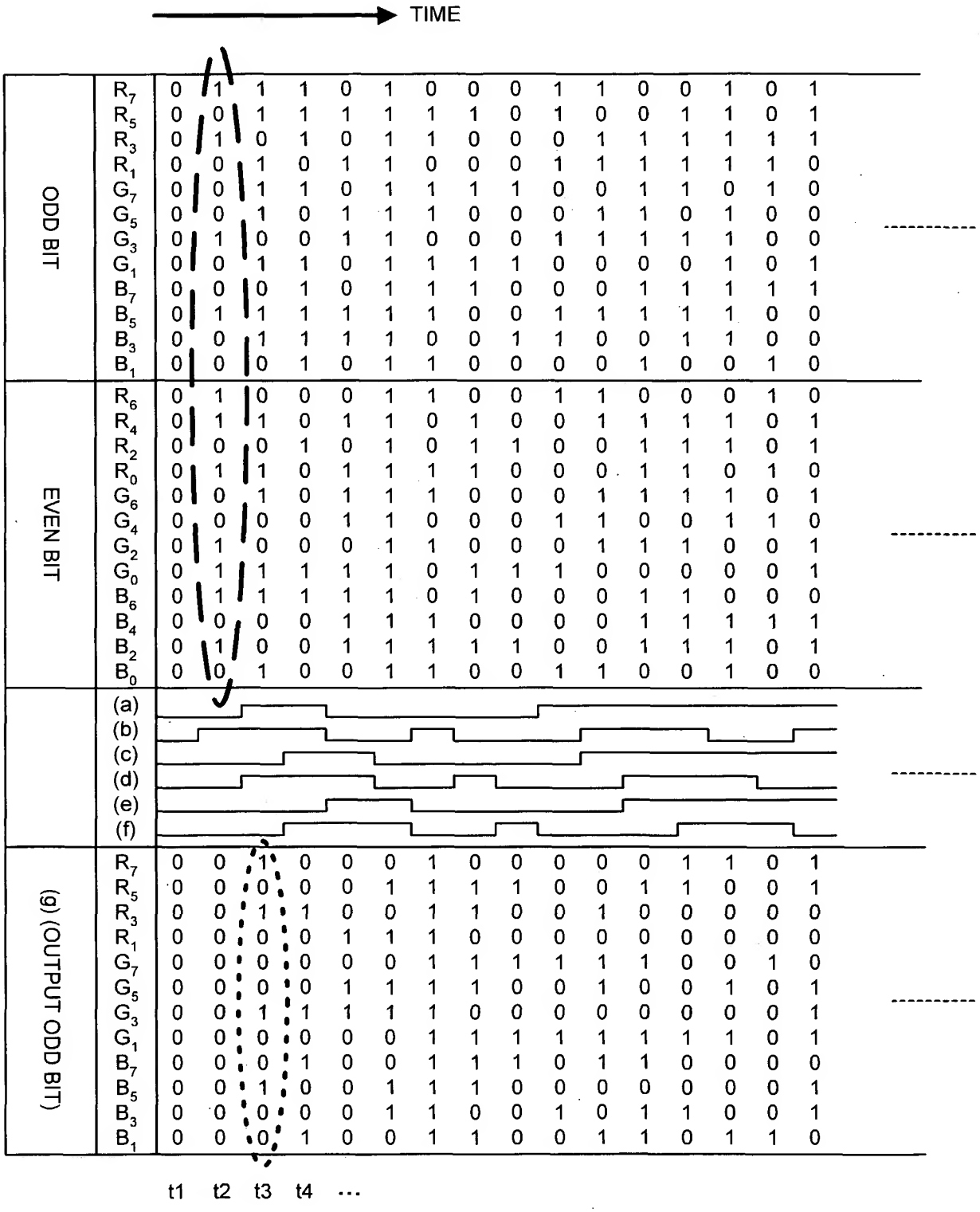
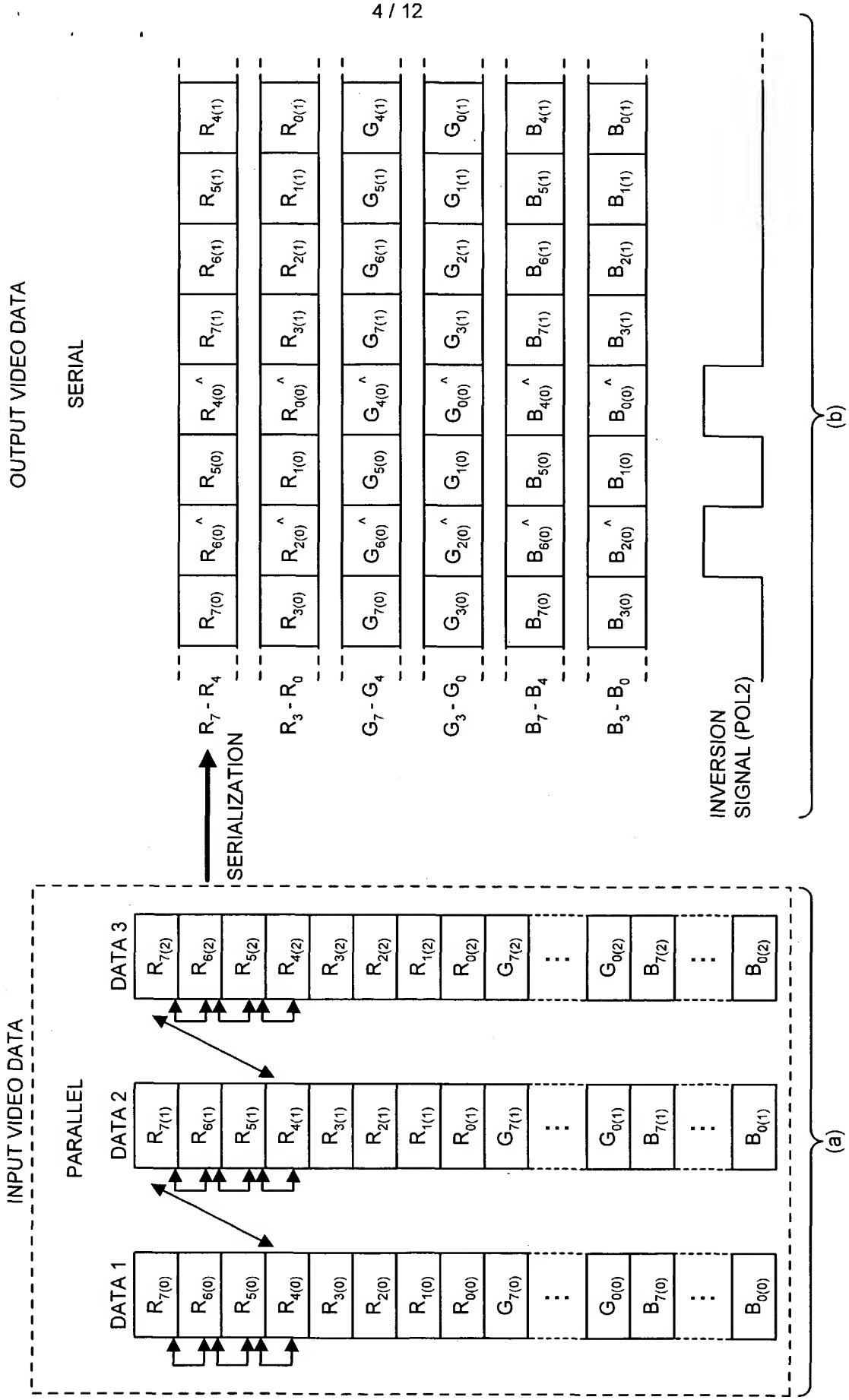

TIME
ODD BIT
EVEN BIT
(g) (OUTPUT ODD BIT)
R7 0 1 1 1 0 1 0 0 0 1 1 0 0 1 0 1
R5 0 0 1 1 1 1 1 1 0 1 0 0 1 1 0 1
R3 0 1 0 1 0 1 1 0 0 0 1 1 1 1 1 1
R1 0 0 1 0 1 1 0 0 0 1 1 1 1 1 1 0
G7 0 0 1 1 0 1 1 1 1 0 0 1 1 0 1 0
G5 0 0 1 0 1 1 1 0 0 0 1 1 0 1 0 0
G3 0 1 0 0 1 1 0 0 0 1 1 1 1 1 0 0
G1 0 0 1 1 0 1 1 1 1 0 0 0 0 1 0 1
B7 0 0 0 1 0 1 1 1 0 0 0 1 1 1 1 1
B5 0 1 1 1 1 1 1 0 0 1 1 1 1 1 0 0
B3 0 0 1 1 1 1 0 0 1 1 0 0 1 1 0 0
B1 0 0 0 1 0 1 1 0 0 0 0 1 0 0 1 0
R6 0 1 0 0 0 1 1 0 0 1 1 0 0 0 1 0
R4 0 1 1 0 1 1 0 1 0 0 1 1 1 1 0 1
R2 0 0 0 1 0 1 0 1 1 0 0 1 1 1 0 1
R0 0 1 1 0 1 1 1 1 0 0 0 1 1 0 1 0
G6 0 0 1 0 1 1 1 0 0 0 1 1 1 1 0 1
G4 0 0 0 0 1 1 0 0 0 1 1 0 0 1 1 0
G2 0 1 0 0 0 1 1 0 0 0 1 1 1 0 0 1
G0 0 1 1 1 1 1 0 1 1 1 0 0 0 0 0 1
B6 0 1 1 1 1 1 0 1 0 0 0 1 1 0 0 0
B4 0 0 0 0 1 1 1 0 0 0 0 1 1 1 1 1
B2 0 1 0 0 1 1 1 1 1 0 0 1 1 1 0 1
B0 0 0 1 0 0 1 1 0 0 1 1 0 0 1 0 0
(a)
(b)
(c)
(d)
(e)
(f)
R7 0 0 1 0 0 0 1 0 0 0 0 0 1 1 0 1
R5 0 0 0 0 0 1 1 1 1 0 0 1 1 0 0 1
R3 0 0 1 1 0 0 1 1 0 0 1 0 0 0 0 0
R1 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0
G7 0 0 0 0 0 0 1 1 1 1 1 1 0 0 1 0
G5 0 0 0 0 1 1 1 1 0 0 1 0 0 1 0 1
G3 0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 1
G1 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0 1
B7 0 0 0 1 0 0 1 1 1 0 1 1 0 0 0 0
B5 0 0 1 0 0 1 1 1 0 0 0 0 0 0 0 1
B3 0 0 0 0 0 1 1 0 0 1 0 1 1 0 0 1
B1 0 0 0 1 0 0 1 1 0 0 1 1 0 1 1 0
t1 t2 t3 t4 ...

FIG. 4


INPUT VIDEO DATA
PARALLEL
DATA 1
DATA 2
DATA 3
SERIALIZATION
OUTPUT VIDEO DATA
SERIAL
R7 - R4
R3 - R0
G7 - G4
G3 - G0
B7 - B4
B3 - B0
INVERSION SIGNAL (POL2)
(a)
(b)

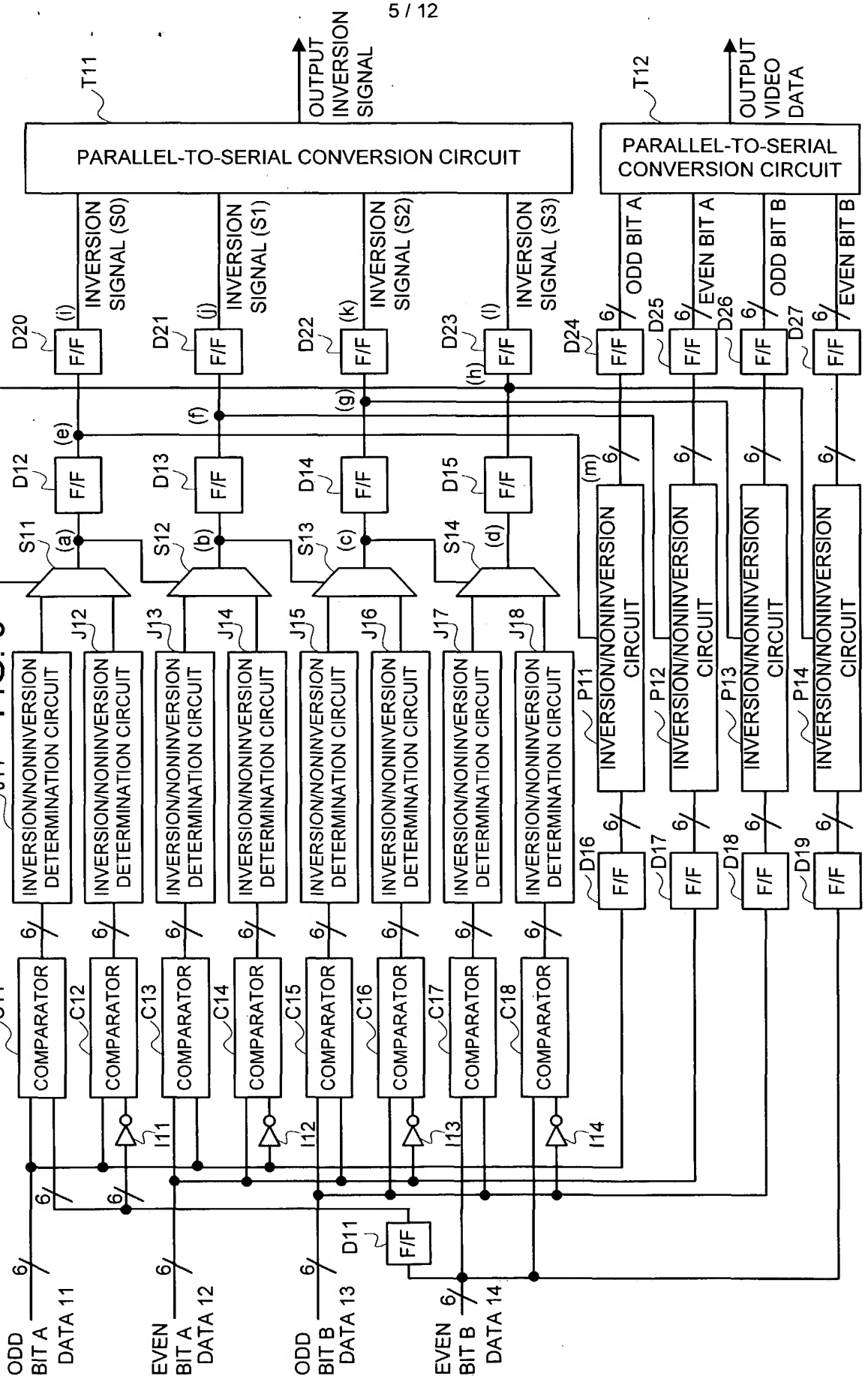

T11
PARALLEL-TO-SERIAL CONVERSION CIRCUIT
OUTPUT INVERSION SIGNAL
T12
PARALLEL-TO-SERIAL CONVERSION CIRCUIT
OUTPUT VIDEO DATA
INVERSION SIGNAL (S0)
INVERSION SIGNAL (S1)
INVERSION SIGNAL (S2)
INVERSION SIGNAL (S3)
ODD BIT A
EVEN BIT A
ODD BIT B
EVEN BIT B
D20
D21
D22
D23
D24
D25
D26
D27
F/F
(i)
(j)
(k)
(l)
(h)
(g)
(f)
(e)
D12
D13
D14
D15
S11
S12
S13
S14
(a)
(b)
(c)
(d)
(m)
J11
J12
J13
J14
J15
J16
J17
J18
INVERSION/NONINVERSION DETERMINATION CIRCUIT
P11
P12
P13
P14
INVERSION/NONINVERSION CIRCUIT
D16
D17
D18
D19
C11
C12
C13
C14
C15
C16
C17
C18
COMPARATOR
I11
I12
I13
I14
D11
6
ODD BIT A DATA 11
EVEN BIT A DATA 12
ODD BIT B DATA 13
EVEN BIT B DATA 14

FIG. 5

FIG. 6

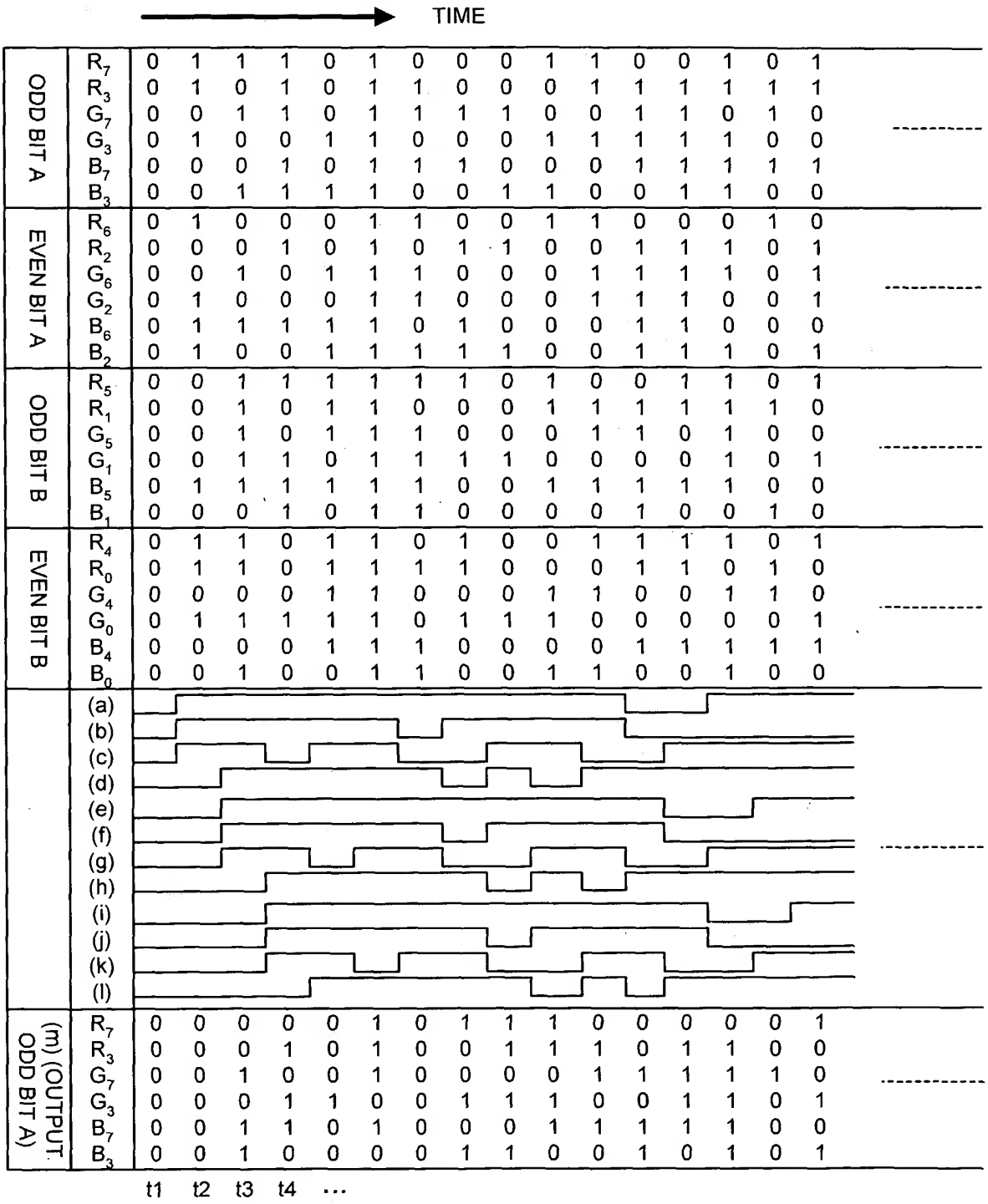

TIME
ODD BIT A
EVEN BIT A
ODD BIT B
EVEN BIT B
(m) (OUTPUT ODD BIT A)
t1 t2 t3 t4 ...

FIG. 7

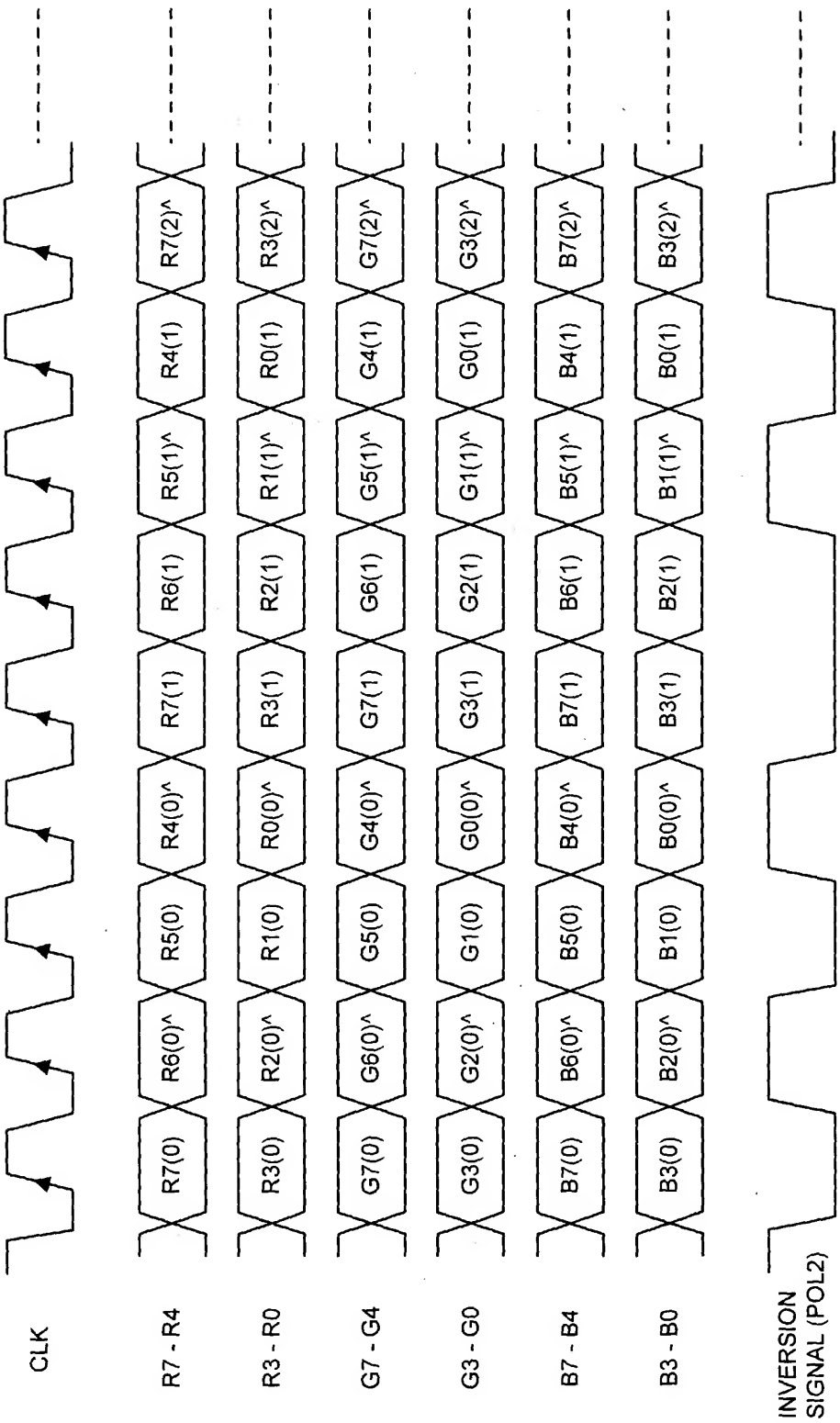

CLK
R7 - R4
R7(0)
R6(0)^
R5(0)
R4(0)^
R7(1)
R6(1)
R5(1)^
R4(1)
R7(2)^
R3 - R0
R3(0)
R2(0)^
R1(0)
R0(0)^
R3(1)
R2(1)
R1(1)^
R0(1)
R3(2)^
G7 - G4
G7(0)
G6(0)^
G5(0)
G4(0)^
G7(1)
G6(1)
G5(1)^
G4(1)
G7(2)^
G3 - G0
G3(0)
G2(0)^
G1(0)
G0(0)^
G3(1)
G2(1)
G1(1)^
G0(1)
G3(2)^
B7 - B4
B7(0)
B6(0)^
B5(0)
B4(0)^
B7(1)
B6(1)
B5(1)^
B4(1)
B7(2)^
B3 - B0
B3(0)
B2(0)^
B1(0)
B0(0)^
B3(1)
B2(1)
B1(1)^
B0(1)
B3(2)^
INVERSION SIGNAL (POL2)

FIG. 8
PRIOR ART

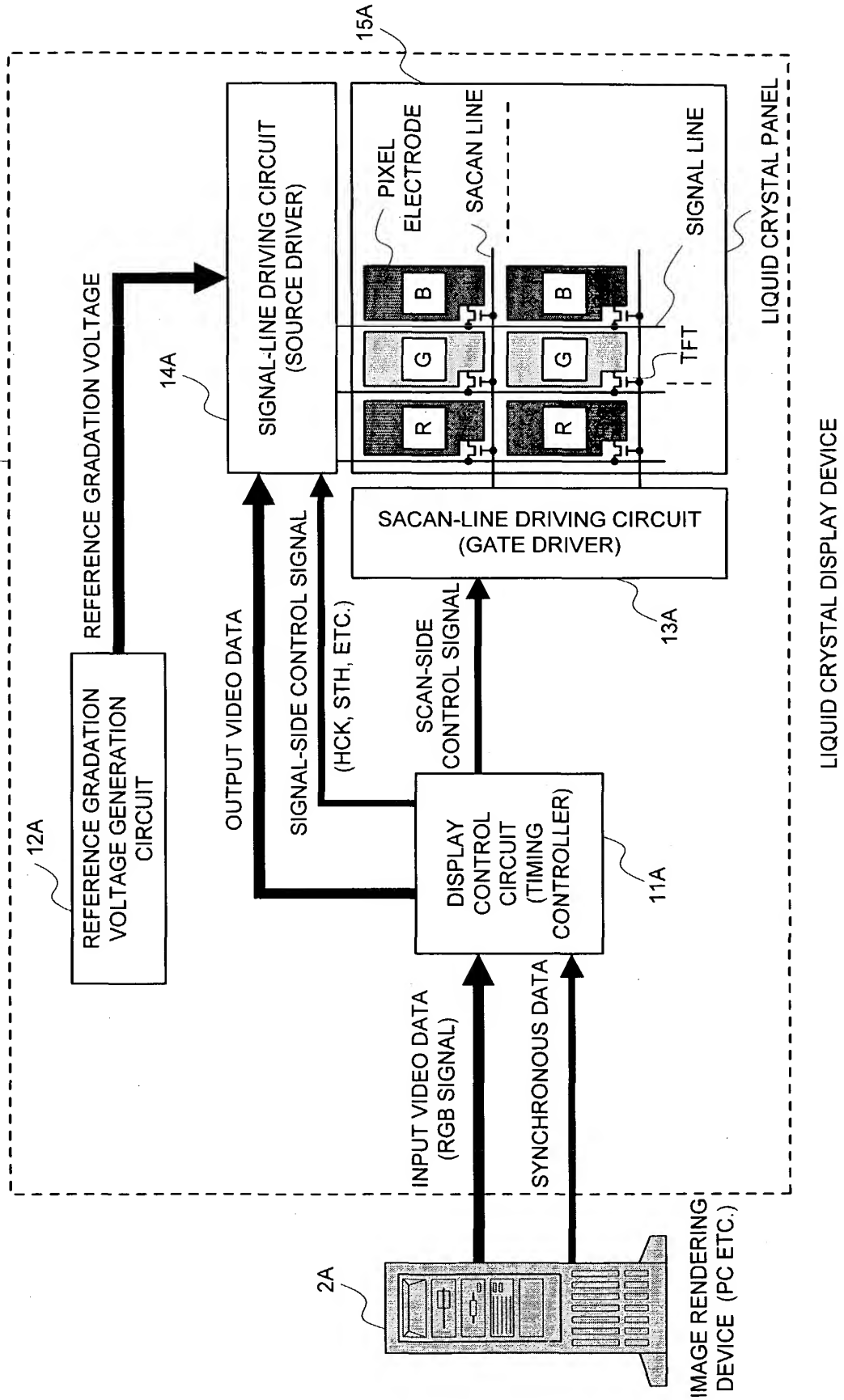


FIG. 9

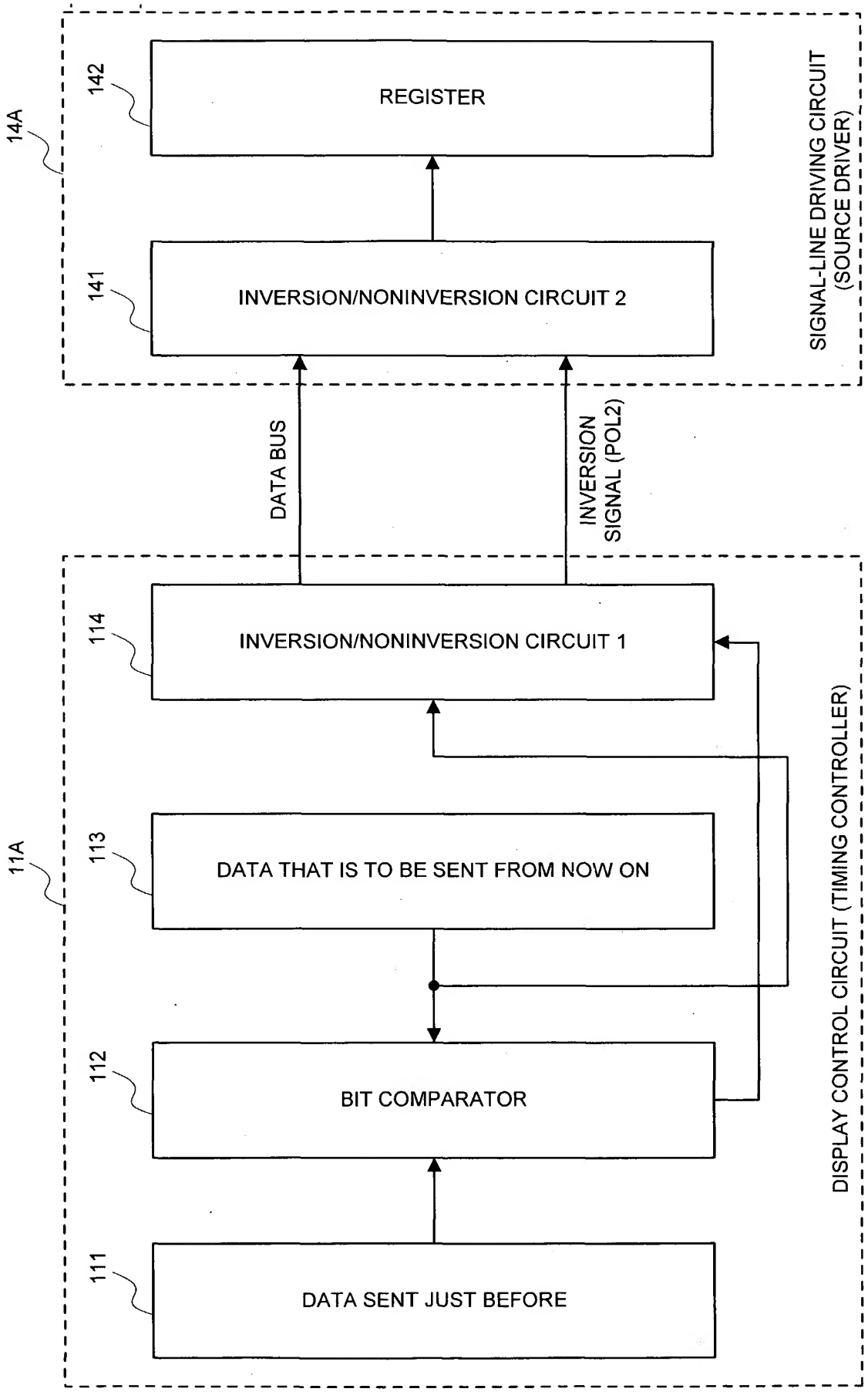

14A
142
REGISTER
141
INVERSION/NONINVERSION CIRCUIT 2
SIGNAL-LINE DRIVING CIRCUIT (SOURCE DRIVER)
DATA BUS
INVERSION SIGNAL (POL2)
11A
114
INVERSION/NONINVERSION CIRCUIT 1
113
DATA THAT IS TO BE SENT FROM NOW ON
112
BIT COMPARATOR
111
DATA SENT JUST BEFORE
DISPLAY CONTROL CIRCUIT (TIMING CONTROLLER)

FIG. 10

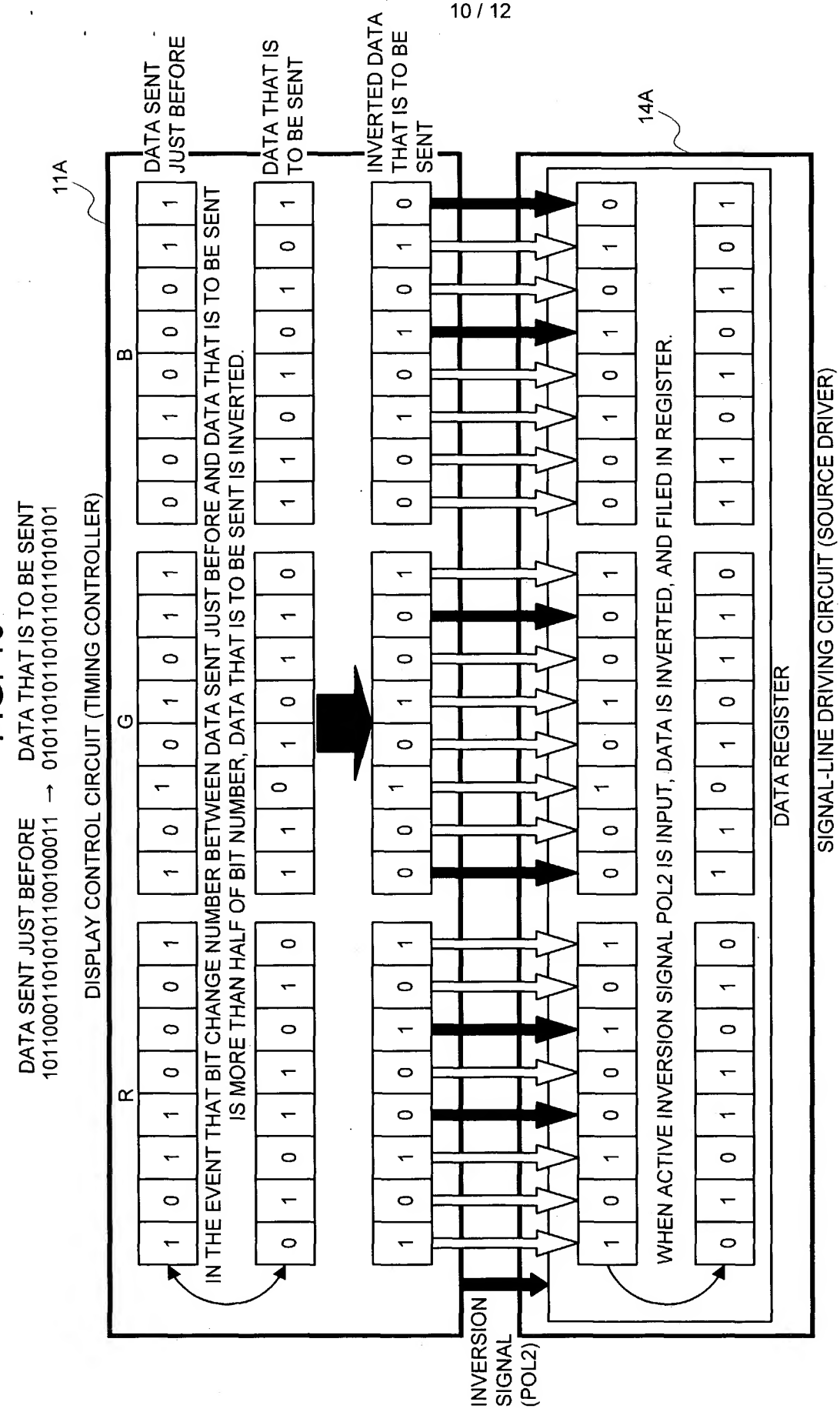

DATA SENT JUST BEFORE
101100011010101100100011
DATA THAT IS TO BE SENT
→ 010110101101011011010101
DISPLAY CONTROL CIRCUIT (TIMING CONTROLLER)
11A
DATA SENT JUST BEFORE
DATA THAT IS TO BE SENT
INVERTED DATA THAT IS TO BE SENT
R
G
B
IN THE EVENT THAT BIT CHANGE NUMBER BETWEEN DATA SENT JUST BEFORE AND DATA THAT IS TO BE SENT IS MORE THAN HALF OF BIT NUMBER, DATA THAT IS TO BE SENT IS INVERTED.
14A
WHEN ACTIVE INVERSION SIGNAL POL2 IS INPUT, DATA IS INVERTED, AND FILED IN REGISTER.
DATA REGISTER
SIGNAL-LINE DRIVING CIRCUIT (SOURCE DRIVER)
INVERSION SIGNAL (POL2)
* SIX DATA BUSES OUT OF 24 ARE SWITCHED.

FIG. 11

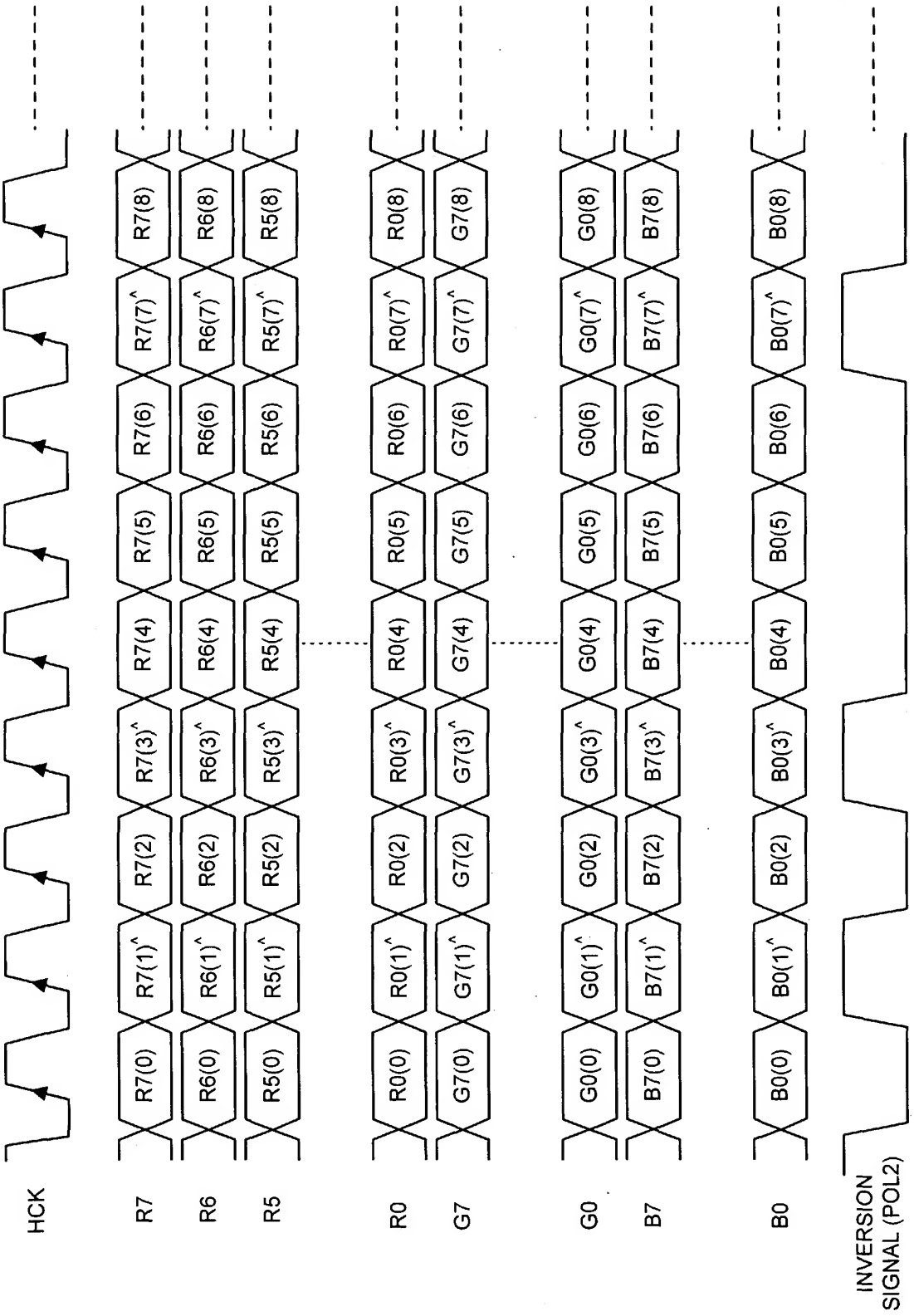
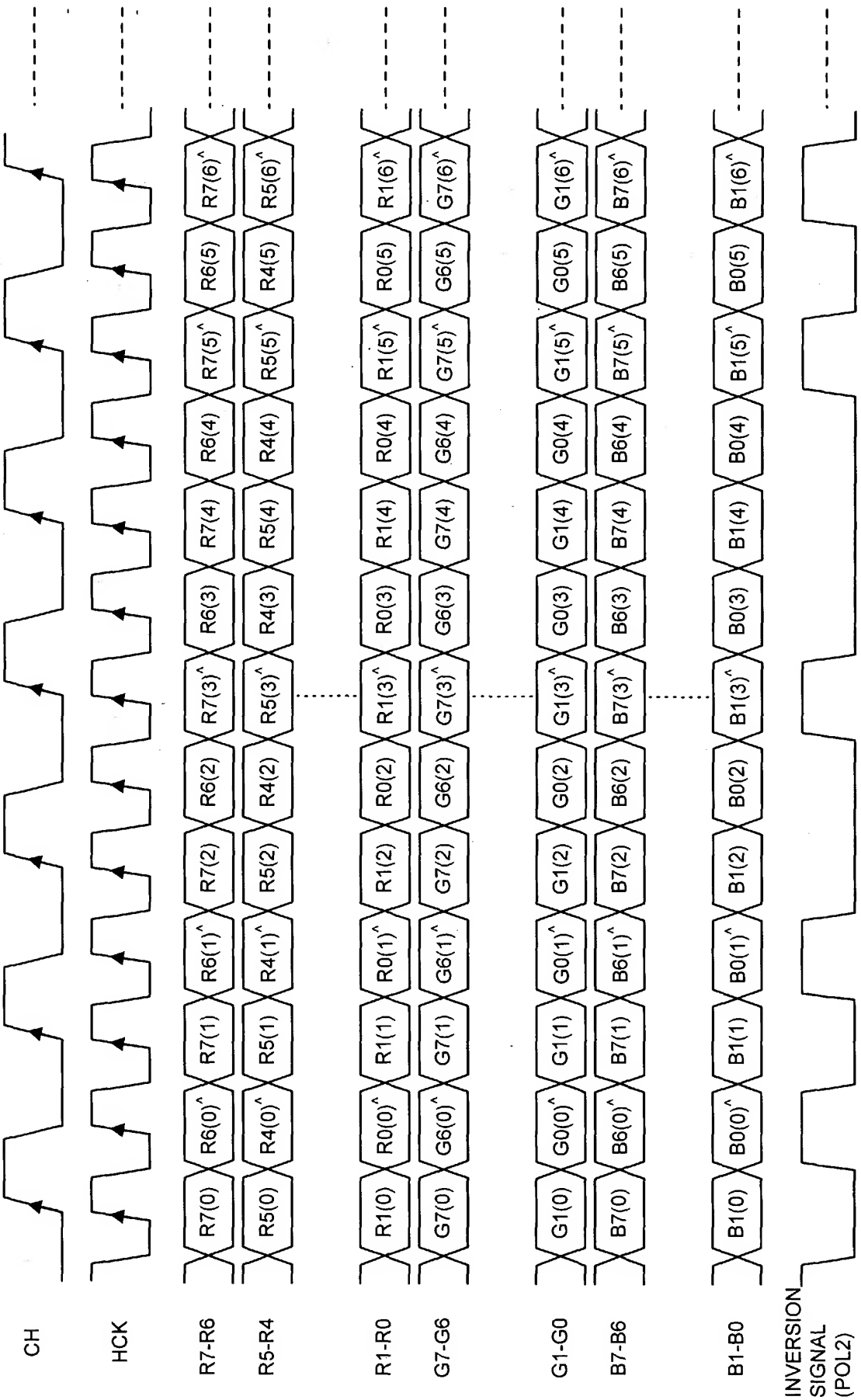

HCK
R7
R6
R5
R0
G7
G0
B7
B0
INVERSION SIGNAL (POL2)
R7(0) R7(1)^ R7(2) R7(3)^ R7(4) R7(5) R7(6) R7(7)^ R7(8)
R6(0) R6(1)^ R6(2) R6(3)^ R6(4) R6(5) R6(6) R6(7)^ R6(8)
R5(0) R5(1)^ R5(2) R5(3)^ R5(4) R5(5) R5(6) R5(7)^ R5(8)
R0(0) R0(1)^ R0(2) R0(3)^ R0(4) R0(5) R0(6) R0(7)^ R0(8)
G7(0) G7(1)^ G7(2) G7(3)^ G7(4) G7(5) G7(6) G7(7)^ G7(8)
G0(0) G0(1)^ G0(2) G0(3)^ G0(4) G0(5) G0(6) G0(7)^ G0(8)
B7(0) B7(1)^ B7(2) B7(3)^ B7(4) B7(5) B7(6) B7(7)^ B7(8)
B0(0) B0(1)^ B0(2) B0(3)^ B0(4) B0(5) B0(6) B0(7)^ B0(8)

FIG. 12


CH
HCK
R7-R6
R5-R4
R1-R0
G7-G6
G1-G0
B7-B6
B1-B0
INVERSION SIGNAL (POL2)
R7(0) R6(0)^ R7(1) R6(1)^ R7(2) R6(2) R7(3)^ R6(3) R7(4) R6(4) R7(5)^ R6(5) R7(6)^
R5(0) R4(0)^ R5(1) R4(1)^ R5(2) R4(2) R5(3)^ R4(3) R5(4) R4(4) R5(5)^ R4(5) R5(6)^
R1(0) R0(0)^ R1(1) R0(1)^ R1(2) R0(2) R1(3)^ R0(3) R1(4) R0(4) R1(5)^ R0(5) R1(6)^
G7(0) G6(0)^ G7(1) G6(1)^ G7(2) G6(2) G7(3)^ G6(3) G7(4) G6(4) G7(5)^ G6(5) G7(6)^
G1(0) G0(0)^ G1(1) G0(1)^ G1(2) G0(2) G1(3)^ G0(3) G1(4) G0(4) G1(5)^ G0(5) G1(6)^
B7(0) B6(0)^ B7(1) B6(1)^ B7(2) B6(2) B7(3)^ B6(3) B7(4) B6(4) B7(5)^ B6(5) B7(6)^
B1(0) B0(0)^ B1(1) B0(1)^ B1(2) B0(2) B1(3)^ B0(3) B1(4) B0(4) B1(5)^ B0(5) B1(6)^